Agenda – Hardware and Signal Processing

Summary of the event

This UDRC Themed meeting will investigate the challenges that are involved in implementing signal processing algorithms into real devices which can then be developed for commercial products.

This meeting will explore challenges and research of signal processing implementation that are ongoing through the UDRC. It will also be an opportunity for the hardware signal processing community to identify synergies, share experiences and views, and to understand Dstl challenges in this important area.

Timings

Tuesday 24th November 2015
9:30 am till 4:30pm

Location

Room R2.15, Royal College Building

University of Strathclyde, 204 George Street, Glasgow G1 1XW

The Royal College Building, is near Queen Street Station in the centre of Glasgow. To find Room 2.15, enter by the Main Door on George Street, walk up to the next level, turn right and R2.15 is at the end of the corridor on the right. Alternatively enter from the side door on Montrose Street and R2.15 is first door on the left.

A map of the campus can be found at
http://www.strath.ac.uk/maps/royalcollegebuilding/

Link to Glasgow City Centre Map
http://www.strath.ac.uk/visiting/gettingtostrathclyde/

Tuesday, November 24, 2015

9:00 am to 9:30 am	***Refreshments and Registration***
9:30 am to 9:40 am	Introduction and Welcome *Dr Stephan Weiss, University of Strathclyde and Prof John Thompson, University of Edinburgh*
9:40 am to 10:25am	Real Time Signal Processing Development for a Through-Wall Passive WiFi Radar *Prof Karl Woodbridge, UCL*
10:25 am to 10.55am	Title tbc *TBC, (Mathworks)*
11:00 am to 11:20 am	***Refreshments***
11:20 am to 11:50 am	LSSC Consortium: Complexity and Cost Reduction of Polynomial EVD Algorithms. *Dr Keith Thompson, LSSC Consortium*
11:50 am to 12:20 pm	Edinburgh Consortium: An overview of Signal Processing Applications and Algorithm Implementations *Dr Calum Blair, Edinburgh Consortium*
12:20 pm to 12:50 pm	Using Dataflow Process Networks for Image Analysis on Heterogeneous Architectures Prof Andrew Wallace, Edinburgh Consortium
12:50 pm to 1:30 pm	***Lunch and Posters***
1:30 pm to 2:00pm	Wideband Processing; the Approach and the Challenges *Richard Streeter, RFEL*
2:00 pm to 2.30 pm	Prizes from previous Themed meeting & Dstl present current challenges from the Hardware and Implementation Signal Processing domain
2.30 pm to 3.30pm	Refreshments available and split into groups to discuss solutions the challenges
3.30 pm to 4.30 pm	Each group presents findings with an open discussion.