University Defence Research Collaboration (UDRC)
Signal Processing in a Networked Battlespace

L_WP5: Low Complexity Algorithms and Efficient Implementation

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Aim: To develop novel paradigms and implementation strategies for a range of complex signal processing algorithms operating in a networked environment. Support all WPs in development of efficient methods and hardware implementations.

Scientifically Possible → Technically Feasible

L_WP5.1 Data reduction and distributed processing

Data Reduction

Lower dimensional representation of data can lead to significant cost reduction. This work will exploit both data dependent and independent techniques (e.g. freq. domain, sub-band or subspace-based processing, thinning of sensor data) and demonstrate low-cost algorithms. Areas of study:

- Polynomial decompositions leading to sparse representations through data-dependent optimal transformations (e.g. Karhunen-Loeve transform), for dimensionality reduction in beamformers.

Distributed Processing

For a networked environment, the efficient organisation of algorithms across a distributed processing platform will be considered (e.g. minimise and set constraints on communications bandwidth between nodes). Areas of study:

- Parallel implementations of linear algebra functions and distributed processing methods (e.g. systolic array design, IP core implementations, vector-codebook methods).
- Statistical signal processing methods (e.g. Bayesian Networks) will be utilised to map algorithms to distributed processors

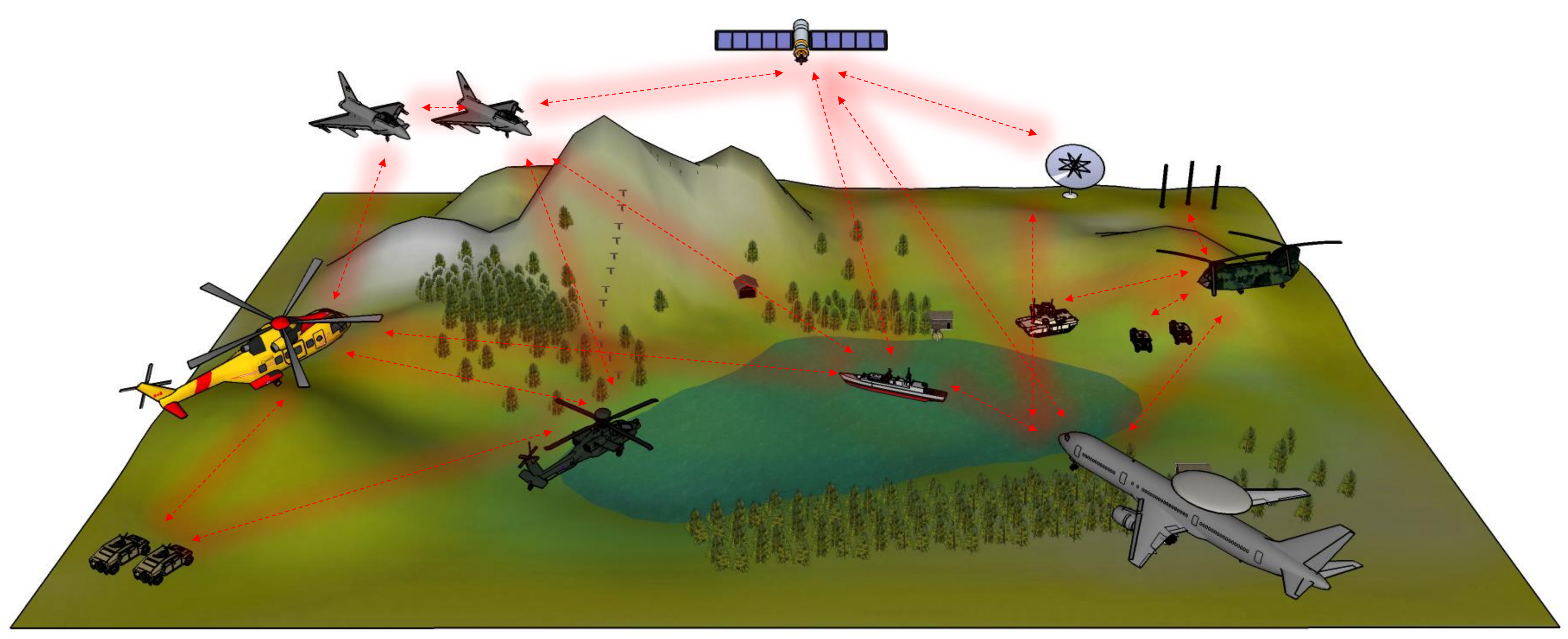
Current Objectives & Progress

Currently investigating the efficient implementation of the SBR2 algorithm [1] to perform Polynomial Eigenvalue Decomposition (PEVD) for Broadband Direction of Arrival estimation. SBR2 has proven costly to implement, with complexity rising quickly with the lag dimension of any polynomial matrix.

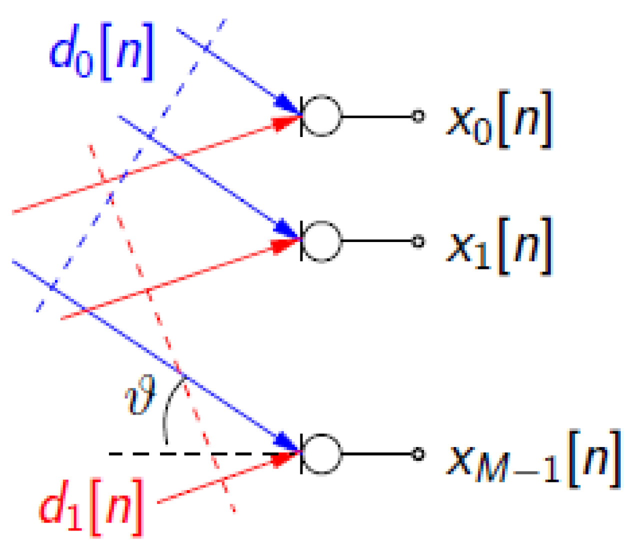
- Matlab Toolbox of optimised software code is in development
- Approximate methods that exploit the growing sparsity of the polynomial matrix upon repeated shift and rotation operations (zero-padding). These 'trim' methods are aimed at limiting the growth of the overall matrix to trade-off efficiency against accuracy.
- Integration of SBR2 with novel 'oversampled sub-band decomposition' methods is under investigation. This concept is to retain coherence between sub-bands, but reduce spectral dynamics within a sub-band, resulting in shorter auto- and cross-correlations.
- Distributed Beamforming – investigations are underway into distributed beamforming techniques, see [2], specifically on how Bayesian Networks [3] can be exploited for message-passing between nodes.
- Distributed Beamformer composed of CubeSat satellite nodes presented at ISP 2013 [4]. This application used a fractal array (sparse) formation of Cubesats to reproduce large antenna behaviour whilst also limiting complexity growth in distributed architecture.

References

[1] J G McWhirter, P D Baxter, T Cooper, S Redif and J Foster. An EVD Algorithm for Para-Hermitian Polynomial Matrices. IEEE Trans Signal Processing, Vol 55, No 6 (May 2007).
[2] Jason Uher, Tadeusz A. Wysocki, and Beata J. Wysocki. Review of Distributed Beamforming. Journal of Telecommunications & Information Technology;2011, Vol. 2011 Issue 1, p78.
[3] Judea Pearl. Probabilistic Reasoning in Intelligent Systems: Networks of Plausible Inference. Morgan Kaufmann (1988).
[4] Karagiannakis, P, Thompson, K, Corr, J, Proudler, I, Weiss, S. Distributed Processing of a Fractal Array Beamformer. Forthcoming IET Intelligent Signal Processing (ISP) Conference, (2013)



Multitude of signals in Networked Battlespace



$$\mathbf{x}_n = \begin{bmatrix} x_0[n] \\ x_1[n] \\ \vdots \\ x_{M-1}[n] \end{bmatrix} = \sum_i \mathbf{s}(\vartheta_i)[n] * d_i[n] + \mathbf{v}[n]$$

$$\mathbf{R}[\tau] = \mathcal{E}\{\mathbf{x}_n \mathbf{x}_{n-\tau}^{\mathrm{H}}\}$$

SBR2 algorithm approximates PEVD of R(τ) Space-time Covariance Matrix for broadband signals

L_WP5.2 Hardware realisations

Collaborating with industrial partners (Mathworks, Texas Instruments, Prismtech), numerically efficient schemes are to be derived. Mappings onto suitable processing platforms are to be investigated that demonstrate real-time algorithms in suitable test scenarios.

- State-of-the-art Multicore DSP/FPGA embedded solutions
- Low power Micro-controllers, DSP and FPGA based processing platforms for inexpensive sensor processing units.
- Multi-core GPU-based platforms and programming environments (such as CUDA) for massively parallel processing of data.
- ARM Based System-on-Chip (SoC) solutions, such as Xilinx Zync, TI OMAP, Nvidia Tegra etc.

Current Objectives & Progress

- Latest FPGA Hardware Development tools assessed
- Academic Symposium 2013 at Texas Instruments
- Show & Tell Event organised for 9th April 2014 – at Strathclyde CMT

Links to other WPs

Collaborative research and active engagement with all other WPs is to result in generic efficient approaches to tackle common themes:

- Dealing with High-dimensional array data
- Identify Parallelization & Distribution Opportunities of Algorithms
- Efficient Uncertainty Analysis
- Developing Efficient Matlab Toolboxes
- Application-specific low-cost hardware implementations

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