On-chip and off-chip processing for high-speed, super-resolution LIDAR

Istvan Gyongy, The University of Edinburgh



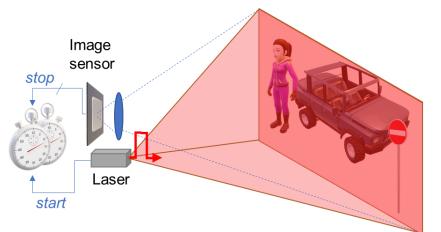
Contents

- Solid-state LIDAR
- SPAD sensor architectures for LIDAR
- Depth map enhancement and scene interpretation

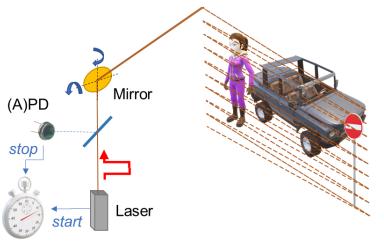




Solid-state



Mechanical scanning

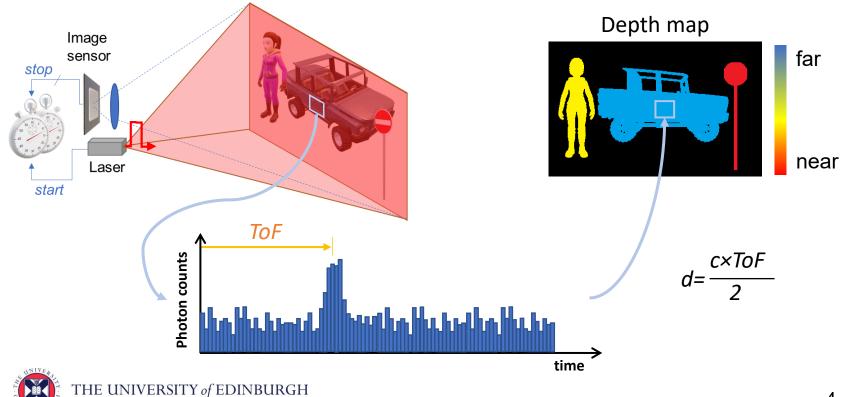


- Compact, robust system ✓
- Lower cost ✓
- Reduced motion artefacts \checkmark



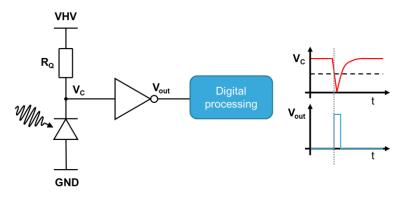
- Simpler receiver architecture <
- Higher SNR ✓

Time-correlated single-photon counting (TCSPC)



Advantages of SPADs

- CMOS-compatible \rightarrow arrays with integrated processing
- Output is digital \rightarrow all-digital receiver
- Low jitter (<100ps) \rightarrow high resolution in z
- Low noise, even at room temp. and above \rightarrow no need for cooling



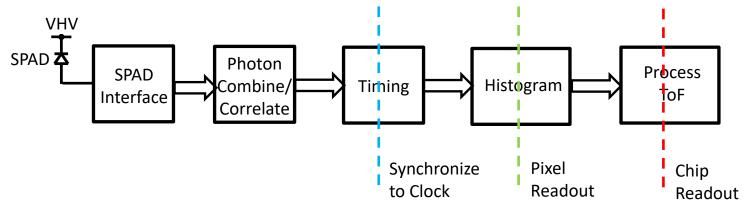


Challenges

- High photon detection efficiency (PDE) (NIR)→ long range (250m)
- High photon throughput → high frame rates even under high ambient levels (100klux)
- Scalable architecture → large FOV with high angular resolution (120°×30°, <0.1°)
- Low power consumption (class 1 laser source)



SPAD ToF Imagers

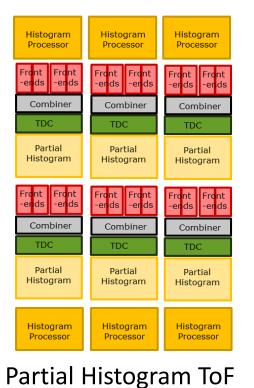


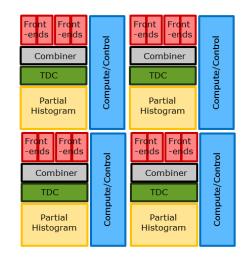
Aim: High resolution, solid-state, scanning/flash imagers for LIDAR

- SPAD Interface (front-end) : quench, buffer, level shift
- Photon Combine : combine or correlate multiple SPADs
- Timing : measure the arrival time of photons
- Histogram : assemble photon event times into a histogram
- Process ToF : Background removal, time of flight fitting, pile-up correction, compress data



3D-Stacked Architectures





Adaptive Histogram ToF

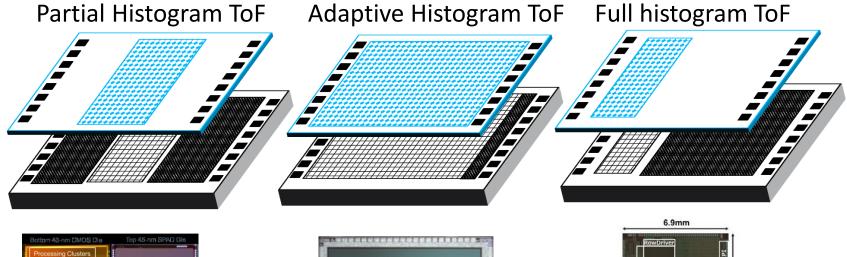
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Combiner			Combiner			Combiner			
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Full histogram ToF



8

Top and Bottom Tier Usage



Processing Clusters Units and Macropixel interface	
80x60 Macropixels Array	320x240 SPAD Array
Processing Clusters Units and Macropixel interface	

Stoppa, IISW 2021

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Zhang, OJSSCS 2021

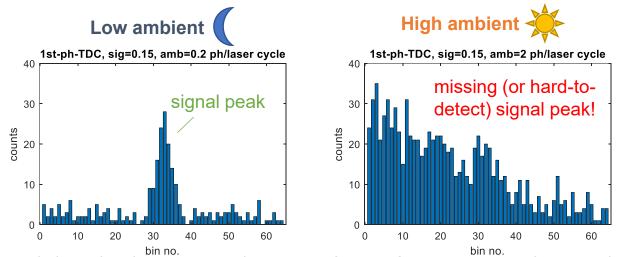
RowOrlver RowOrlver frontend DSP PLL Por Bottom layer

Kumagai, ISSCC 2021



First photon TDC

• Traditional single-photon LIDAR systems use "first-photon" time-to-digital converters (TDCs) which register only the first photon event per laser cycle and frame

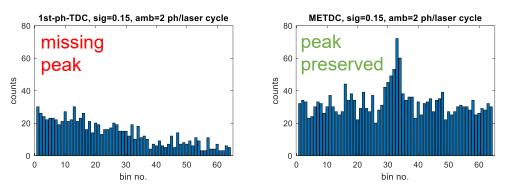


• The approach breaks downs, resulting in **pile-up distortion**, as the number of photon detections/TDC channel/laser cycle approaches 1



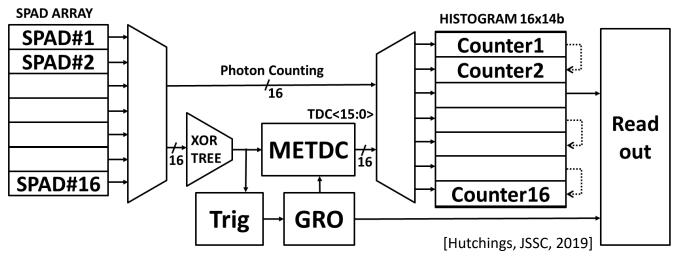
Mitigating TDC pile-up

- **Coincidence detection** (e.g. [Beer, 2018]) which filters photon events in an attempt to ensure that only "signal" events are processed by the first-photon TDC
- Time gating (e.g. [Padmanabhan, 2021])
- Multi-event histogramming TDC (e.g. [Hutchings, 2019]) which registers multiple events per laser cycle and builds a histogram over multiple cycles





Multi-event Histogramming (Quantic4x4)

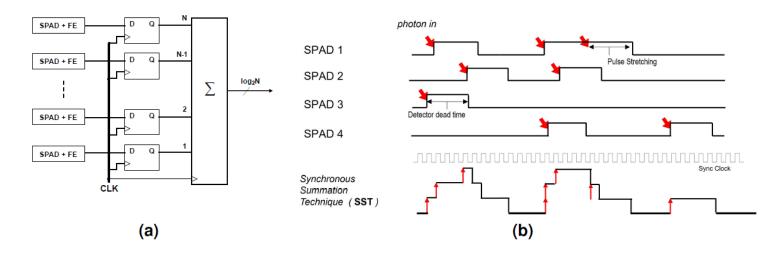


- 4x4 sharing of shift register-based Multi event TDC
- 16x14b bins, 560ps/bin
- Good background tolerance
- Other implementations:

[Van Blerkom, ISSW, 2020], [Seo, JSSC 2021], [Srowig, ISE, 2022]



Synchronous Summation Technique (SST)



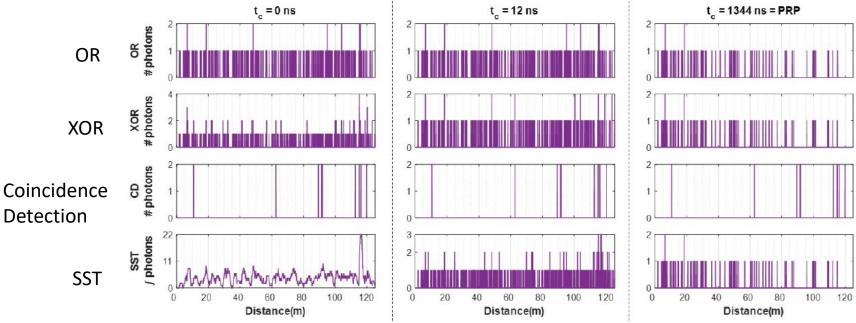
[Patanwala, PhD Thesis, U. Edinburgh, 2021]

- SST combines readily with a multi-event TDC operating on CLK
- Pipelined TDC operation required for faster clock rates
- Modelling/emulated comparison with OR, XOR and coincidence combining



Synchronous Summation Technique (SST)

Simulated histograms: 115m range, 100kLux ambient, 10% reflectivity target

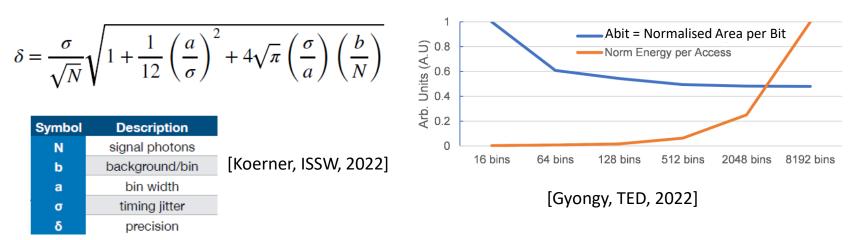


[Patanwala, PhD Thesis, U. Edinburgh, 2021]

Only SST + short conversion time t_c able to recover target

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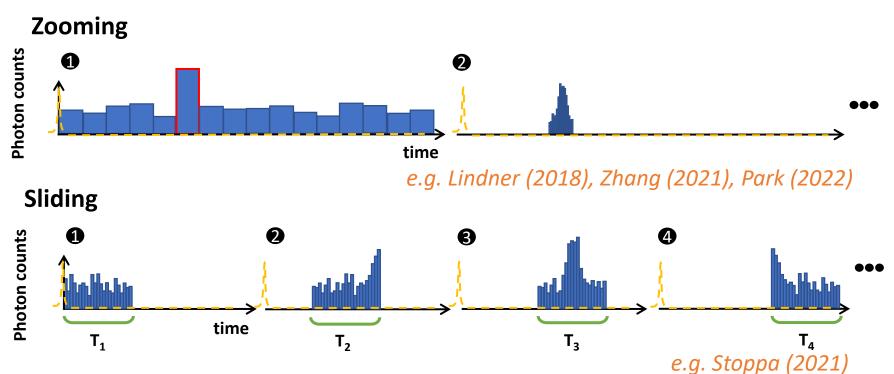
How many histogram bins?



- Choose bin width *a* to be around laser IRF FWHM
- Few 100ps and 100's bin for short range (0-10m) flash LIDAR
- Few ns and 1000's bins for long range scanning/flash (50-300m) LIDAR
- Large SRAM histogram has energy overhead
- Smaller SRAM histogram has high access logic overhead counters better

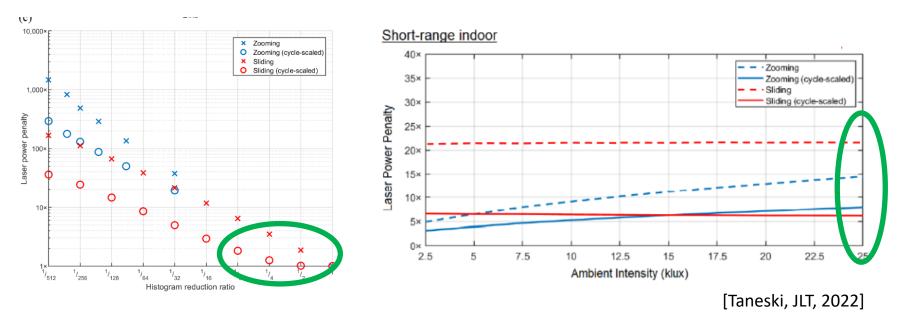


Partial Histogramming



• Only subrange of full depth held in pixel THE UNIVERSITY of EDINBURGH

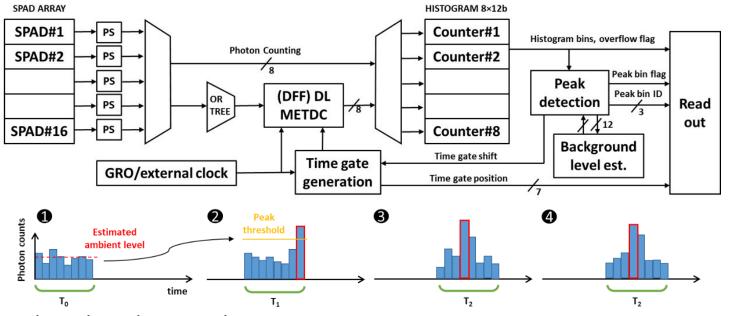
Partial Histogram – Power Penalty



- Histograms of 1/4-1/8th full scale depth range provide acceptable compromise
- Scaling laser cycles with sub-range can save significant emitter power



Partial Histogram – peak tracking (HSLIDAR)



• Pixels with multi-event histogramming

[Gyongy, ISSW 2022]

- Peak tracking in pixel with in-pixel background estimator
- Dynamic vision mode outputs only pixels with change in depth THE UNIVERSITY of EDINBURGH

HSLIDAR – peak tracking

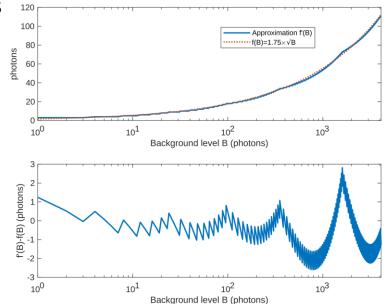
Peak detection threshold is calculated as

 $h_{thresh} = B + 1.75\alpha\sqrt{B}$

where *B* is the estimated background level and $\alpha = 1$ or 2.

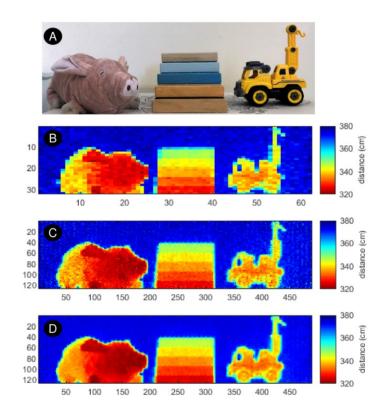
A direct time-of-flight image sensor with in-pixel surface detection and dynamic vision

Istvan Gyongy, Ahmet T. Erdogan, Neale A.W. Dutton, *Member, IEEE* Germán Mora Martín, Alistair Gorman, Hanning Mai, Francesco Mattioli Della Rocca, *Member, IEEE* and Robert K. Henderson, *Fellow, IEEE*





HSLIDAR – short range



Single frame (1kFPS) (bin width = 8 ns)

HR: Combination of 16 frames (20FPS)

Average of 20 HR images



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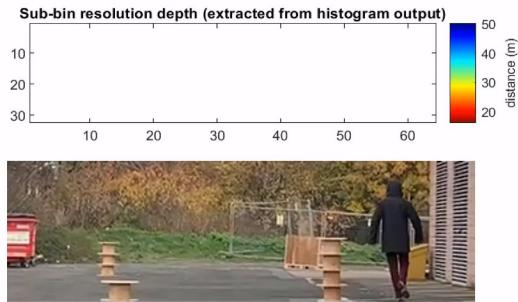
Partial Histogram – peak tracking





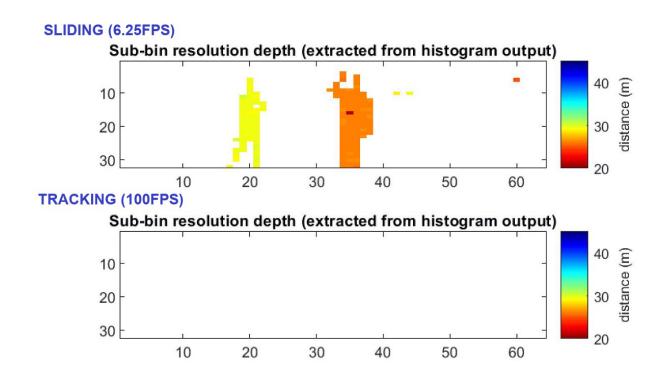
Partial Histogram – peak tracking

TRACKING (100FPS)



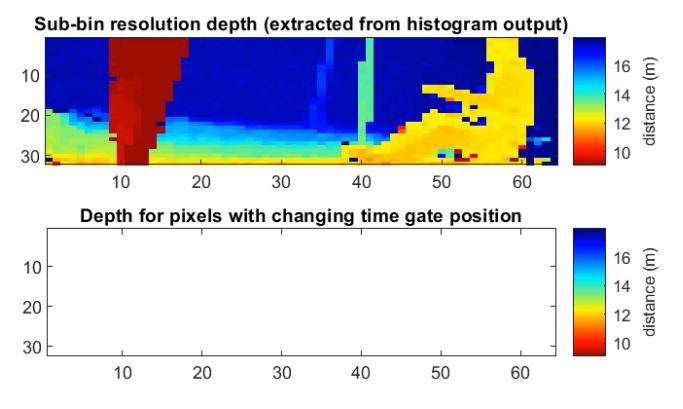


Sliding vs peak tracking



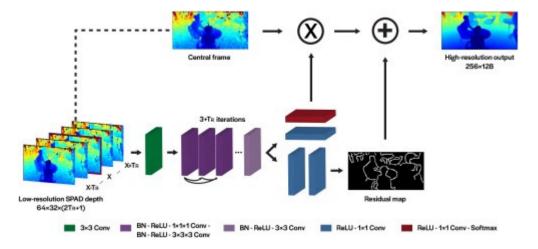


Dynamic vision using peak tracking





Depth upscaling



1

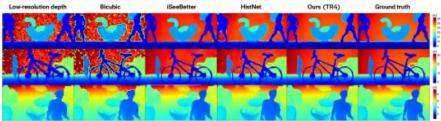
2

3

Research Article	Vol. 31, No. 5/27 Feb 2023/ Optics Express 7060
Optics EXPRESS	

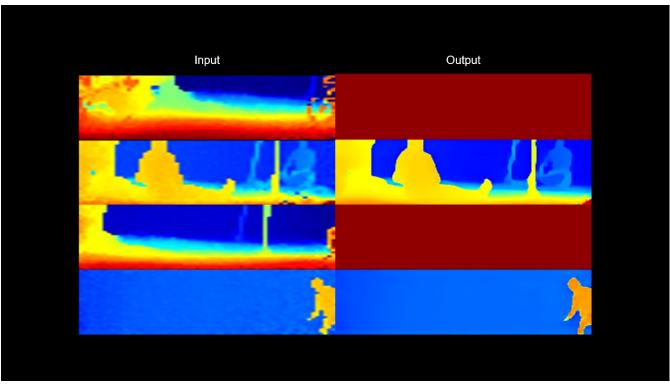
Video super-resolution for single-photon LIDAR

Germán Mora-Martín, 1,* (b) Stirling Scholes, 2 Alice Ruget, 2 Robert Henderson, 1 (b) Jonathan Leach, 2 and Istvan Gyongy 1





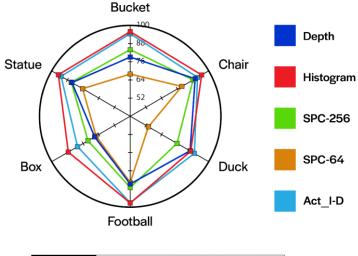
Depth upscaling (cont.)





High-speed object detection

F1 score



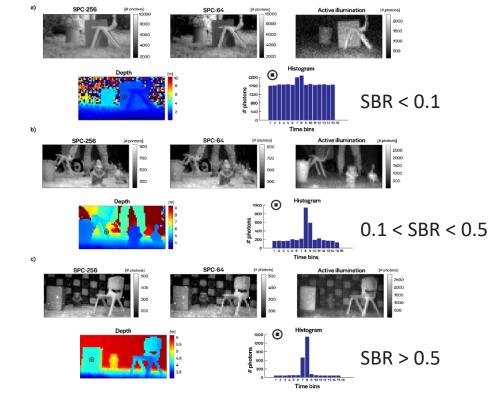
Research Article	Vol. 29, No. 21/11 Oct 2021 / Optics Express 331
Optics EXPRESS	

High-speed object detection with a single-photon time-of-flight image sensor

GERMÁN MORA-MARTÍN,^{1,*} ALEX TURPIN,^{2,3} ALICE RUGET,⁴ ABDERRAHIM HALIMI,⁴ ROBERT HENDERSON,¹ ⁽⁵⁾ JONATHAN LEACH,⁴ AND ISTVAN GYONGY¹ ⁽⁵⁾

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Reconfigurable/Neural Net Processing

- Processor under the SPAD array [Ardelean, PhD Thesis, EPFL, 2023]
- Higher-level (AI) processing for scene interpretation akin the 2D vision sensors?

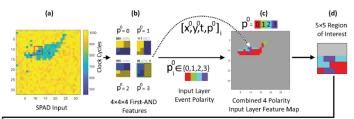


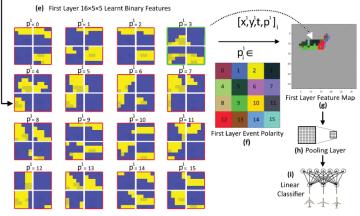
Source: https://www.sony-semicon.com/



Reconfigurable/Neural Net Processing (cont.)

- SPAD array with on-chip logic to generate events depending on order that neighbouring SPADs fire
- Overlapping "receptive fields" with 4×4 SPADs
- 81 fold reduction in data rate
- Asynchronous readout to FPGA with spiking neural network for object classification





[S. Afshar, IEEE Sensors 2020]



Conclusions

- Recent advances in stacked 3D SPAD technology have resulted in high PDE SPADs, and enabling focal-plane photon processing in advanced technology nodes
- There is still a lot of opportunity for circuit and system innovation to address angular resolution, power reduction and dynamic range challenges, especially in longer-range LIDAR
- In the coming years, we are likely to see more sophisticated embedded processing, including programmable logic, machine learning, and SNNs.



Acknowledgements

- Robert Henderson, Jonathan Leach, Abderrahim Halimi, Germán Mora-Martín, Alex Turpin, Alice Ruget, Stirling Scholes, Ahmet Erdogan, Neale A.W. Dutton, Alistair Gorman, Hanning Mai, Francesco Mattioli Della Rocca
- Robert Henderson for slides from ESSCIRC 2022 tutorial "3D stacking meets 3D imaging: Vertically Integrated SPAD Sensor Architecture" (material used on slides 7-9 and 12-17 here)
- STMicroelectronics for chip fabrication, PhD sponsorship
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